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GENERIC ENGINEERING FORMATS FOR ELECTRONIC PINOUT INTERFACE CHARACTERISTICS OF DIGITAL BOARD/ASSEMBLY TESTERS

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This report documents the development of a set of generic engineering formats for the characterization of performance parameters at the interface at an advanced digital board test systems on a pin by pin basis. The parameters of concern here are input and output data lines, clocks and control lines. The emphasis of this effort has been to identify enough of the pertinent parameters to enable a "Congruent Match" between different testers with the same capability at the Hardware Interface Level.

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EXECUTIVE SUMMARY

This technical report is a mechanism for documenting the performance of a generic high performance test system considered from a behavioral (look alike) approach. The tester's high speed digital test interface is considered from the perspective of the technology of the stimulus/response/control electronics involved. Such a systematic approach attempts to quantify those technical requirements needed to know the bounds of system capability.

The pin characterization format sheets included herein provide a detailed list of parameters appropriate to a wide variety of functions typically performed by an array of tester pins for a digital circuit board or group of boards or at the next replaceable assembly level.

The specifics contained herein represent the results of numerous discussions with TPS development engineers of extensive experience with digital ATE over a period of more than 25 years. They cover capabilities ranging from the earliest sequential I/O-type testers, circa 1970, to modern DTUs such as that used in CASS, and include some characteristics intended to respond to currently foreseen technologies such as the high-speed bus.

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1.0 INTRODUCTION

1.1 The purpose of this report is to document the development of a set of generic formats for the characterization of pins in an advanced digital functional test system. The digital pins of concern here are Inputs, Outputs, Output Clocks, External Input Control lines and External Input Clocks. The emphasis of this study has been to identify enough of the pertinent parameters among all of the possible parameters to enable a "Congruent Match" between different testers with the same capability at the Hardware Interface Level. This should greatly assist in:

a. determining the suitability of the defined test system for a particular application or,

b. providing a convenient mechanism for the comparison and analysis of present and future test Systems with each other and eliminating the confusion of jargon and subtlety of contradictory terminology and definitions used by different manufacturers.

In summary, the intent is to provide a convenient brief, technically concise portrayal of the Digital Test capability of a given test system.

1.2 Chapter 2 of this report contains the methodology of how the report was prepared and some of the tradeoffs made to keep the effort manageable.

1.3 Chapter 3 contains the developed format for digital output signals, Chapter 4 contains the format for digital input signals, Chapter 5 for control lines and Chapter 6 for clocks. In addition, each format is accompanied with a table showing each category of data called out in the format, what each function or data item addresses, and the reason or requirement for that particular data item.

1.4 Chapter 7 is a glossary of terminology as it applies to the report.

1.5 Chapter 8 contains Observations and Conclusions that evolved during the generation of this report.

2.0 METHODOLOGY

2.1 This report is the result of a review of commercial and military ATE manuals, Test Requirements Documents, Specifications and other related documentation ranging from the early military Automated Test Equipment (ATE) such as VAST and commercial test equipment such as the GenRad 1790 (circa 1970) up to the Navy's present day CASS (Consolidated Automated Support System) and other commercially available ATE. In addition, a brief analysis of future technological needs was also included. Both functional and In-circuit, and Very Large Scale Integrated (VLSI) test systems were reviewed to eliminate a bias towards particular UUTs or applications. Also utilized were the results of two prior studies conducted by independent consultants as well as additional research and a number of discussions with personnel from Naval Air Warfare Center, Aircraft Division (NAVAIRWARCENACDIV), Lakehurst, NJ and NAVAIRWARCENACDIV, Patuxent, MD. The results of these reviews, studies, and discussions were distilled into a set of data capture formats. These formats, although comparatively thorough, were somewhat unwieldy as they addressed parameters that were internal and were not necessarily evidenced at the ATE interface, or, difficult to obtain without special purpose test equipment. These formats were reviewed at several different meetings with cognizant technical personnel at NAVAIRWARCENACDIV, Patuxent River and forged into a more practical product. These results were then in turn tailored and modified into the final product of this report.

2.2 In this entire process there was a continual conflict between the totality of all the possible parameters versus what is significant and practicable to obtain. For example, one would like to know parameters associated with ringing, ground bounce, forward crosstalk and impedance reflection but these would be difficult and expensive to obtain at the DTU interface. Our compromise here is to lump all these parameters under quiescent noise. Another situation like this is the master clock frequency, and related parameters that help determine much of the DTU's inherent timing capabilities. Unfortunately these signals are not necessarily available at the interface, and therefore could not be included. The formats developed in this report are not a representation of all the parameters but they are as good or somewhat better than the best commercial specifications that are presently available. They are adequate to give a very tight match between a UUT and a Tester or a Tester vs Tester comparison.

2.3 The characterization of signals in this report addresses as a minimum:

a. Semiconductor technology, waveform parameters such as rise and fall-times, voltage threshold levels, and shielding.

b. Clock Rates, clock logic definitions and relationships to signals such as setup and hold times, and dynamic timing in general.

c. Transmission line and interconnect characteristics between the UUT and test fixturing as well as between the ATE electronics and its interface.

d. Digital data line flexibility in the sense of handling bi-directional, multiplexed signal busses already seen in profusion in nearly all digital electronic circuitry.

e. Digital information definitions with inherent protocols such as MIL-STD-1553.

Also considered were the definitions of Impedance, propagation delay, signal levels, cross-talk, etc. The objectives were to support both the **dynamic** and **static** digital test environment with appropriate and unambiguous terminology which are contained in the report glossary for the most popular technologies likely to be encountered in current and near-term advanced military testing.

3.0 DIGITAL TESTER OUTPUT CHARACTERISTICS

This section covers the specific format developed for the digital, test or output characteristics, see Figure 1. All testers need to address items A through D on the format sheet. Where a specific item would not be applicable, for instance Hi-z may not be applicable for all testers simply state N/A. Most but not all testers need to address E "Memory". Only dynamic testers need to address item F "Dynamic Characteristics" the remainder of the chapter is back up data that supports each of the items in Figure 1. The term "CATEGORY" addresses a specific item in Figure 1. The term "FUNCTION" addresses what does the parameter or item do and "REQUIREMENT/REASON" addresses why one would want to know or obtain that piece of information.

GPI PIN NO (S)

OUTPUT

FIGURE 1 – DIGITAL TESTER OUTPUT CHARACTERISTICS

A INTERFACING

1. TYPE
   - a. Single ☐
   - b. I/O ☐
   - c. Dynamic ☐
   - d. Static ☐

2 Delays in nanoseconds

Parameter	Value
a. Skew - Pin/Pin same card	
b. Skew - Pin/Pin different card	
c. Gated Clock Out This Pin	
d. Ext Clock In to This Pin	
e. Ext Trigger In to This Pin	
f. Delay Inst to I/O	

3 Shielding

a. Shielding

(1) Yes ☐
(2) No ☐
Check only one

- b. Shielded and grounded at DTU ☐
- c. Shielded and grounded at I/F ☐
- d. Coax and grounded at DTU ☐
- e. Coax and grounded at I/F ☐
- f. Twisted Pair ☐

4 Boundary Scan

a. Yes ☐ b. No ☐

B TECHNOLOGIES

Check all that apply

		Drive	
[illegible]			
MOS			
CMOS			
[illegible]			
ECL			
[illegible]			
[illegible]			
[illegible]			
BIPOLAR			
HYBRID			

C DC LEVELS

1. Voltage Levels

Parameter	Value
a. High Range	
(1) V Out High	
(2) V Out Low	
b. Low Range	
(1) V Out High	
(2) V Out Low	
c. Accuracy	
d. Resolution	
e. V Swing	

2. Current Levels

Parameter	Current
a. Drive Hi	
b. Drive Lo	
c. Leakage Hiz	

3. Impedance

Parameter	Imp
a. Out Drive Hi	
b. Out Drive Lo	
c. Out Hiz (off)	
d. Worse Case	

D OPERATIONAL LIMITS

1. Tri-State Drive	Yes	NO
a. On The Fly		

2. Slew Rates	
a. Maximum	
b. Minimum	

3. Voltages	
a. Max Voltage at Max Data Rate (unmultiplexed)	
b. Max Voltage at Max Data Rate (multiplexed)	

4. Data Rate Gen	
a. Has DRG	
b. Doesn't have DRG	
Parameter (unmultiplexed)	
c. Minimum Data Rate External Trigger	
d. Minimum Data Rate	
e. Max Data Rate	
f. Max Data Rate External Trigger	
g. Max Data Rate at Max Voltage	
h. Resolution	
i. Accuracy	
j. Jitter	
Parameter (multiplexed)	
k. Minimum Data Rate External Trigger	
l. Minimum Data Rate	
m. Max Data Rate	
n. Max Data Rate External Trigger	
o. Max Data Rate at Max Voltage	
p. Resolution	
q. Accuracy	
r. Jitter	

E MEMORY

1. Pin Pattern Memory
   - a. Pin Memory yes ☐ no ☐
   - b. Ram Depth
2. Store Method
   - a. Not Applicable ☐
   - b. Exp vs Actual (1) ☐
   - Detected State (2) ☐
   - c. With Mask (1) ☐
   - Without Mask (2) ☐
   - d. Signature Analysis (3) ☐
3. Pattern Generator
   - Algorithmic (1) ☐
   - a. Ram (2) ☐
   - Direct (static only) (3) ☐

F DYNAMIC CHARACTERISTICS

1. Formatter selectable to
   - a. DTU ☐ (1)
   - CARD ☐ (2)
   - PIN ☐ (3)

b. Types (unmultiplexed)

- NR ☐ (1)
- RI ☐ (2)
- SBC ☐ (3)
- RZ ☐ (4)
- RO ☐ (5)
- RTC ☐ (6)

c. Types (multiplexed)

- NR ☐ (1)
- RI ☐ (2)
- SBC ☐ (3)
- RZ ☐ (4)
- RO ☐ (5)
- RTC ☐ (6)

2. Timing Gen Due for each
   - a. DTU (1)
   - CARD (2)
   - PIN (3)
   - b. Timing Sets
   - c. Stimulus /periods/set
   - d. Clocks per set

Timing Parameter	(1) Min	(2) Max	(3) Res	(4) Acc
e. Pattern Period				
f. Stim Period Begin				
g. Stim Period End				
h. Stim Period Width				
i. Stim Period on/off				

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS

CATEGORY	FUNCTION	REQUIREMENT/REASON
A. INTERFACING 1. Type a. Single [] b. I/O []	Address whether pin is single dedicated or bi-directional	1. Show if a pin is bi-directional; if it can handle busses 2. Other functions of pin must be covered by formats elsewhere
c. Static [] d. Dynamic []	Addresses basic capability of tester	Delineates whether tester has signal formatting and/or time placement capability
2. Delays a. Skew - Pin/Pin (Same Card)	Specifies delays between pins of same tester card	Address if UUT can tolerate inherent delays between pins on tester
b. Skew - Pin/Pin (Diff Card)	Specifies delays between pins on different tester cards	Address if UUT can tolerate inherent delays between pins on tester
c. Gated Clock out this pin	Specifies time between gated clock out of tester and tester output pin	Synchronization of critical timing between DTU and UUT
d. Gated clock into this pin	Specifies time difference between external clock input to DTU and DTU pin output	Synchronization of critical timing between DTU and UUT
e. External Trigger to this pin	External trigger to turn output pin either on or off	Critical timing considerations when UUT requires a response from DTU

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
f. Delay inst to I/O	Delay in nanoseconds between the DTU and station I/O	A factor to be considered in TPS design when critical timing is a factor
3. Shielding a. Shielded (1) Yes [] (2) No []	Reduces susceptibility to outside stimulus and interference	Tester would be severely limited to perform adequately above 10 Mhz
b. Shielded and grounded at DTU []	Provides good signal grounding fidelity up to approx 20 Mhz	Required for shielding design in ID
c. Shielded and grounded at I/F []	Provides good signal grounding fidelity up to approx 20 Mhz	Required for shielding design in ID
d. Coax and grounded at DTU []	Provides good signal grounding fidelity above 20 Mhz up to GHz range	Required for hi-speed signal interconnect to ID
e. Coax and grounded at I/F []	Provides good signal grounding fidelity above 20 Mhz up to Ghz range	Required for hi-speed signal interconnect to ID
f. Twisted Pair []	Inexpensive shielding method valid to approx. 10 Mhz	Required for interconnect matching into ID
4. Boundary Scan (a) Yes [] (b) No []	Tester specifically does or does not have a boundary scan capability (protocols and deep memory > 1 Meg)	Some newer designs make extensive use of this capability
B. TECHNOLOGIES	Identifies specific logic characteristics (voltages,currents, impedances)	Identifies specific operating parameters required during testing

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
C. DC LEVELS a. High Range 1. Vout high	Max programmable DC voltage of logic 1	Upper voltage
2. Vout low	Min programmable low voltage of logic 1 range	Lower voltage limit of logic 1 output range
b. Low Range 1. Vout high	Max programmable DC voltage of logic 0 range	Upper voltage limit of logic 0 output voltage range (Must be less than logic 1 value)
2. Vout low	Min programmable DC voltage of logic 0 range	Lower limit of logic 0 output voltage range (Must be less than logic 1 value)
c. Accuracy	Accuracy of program vs actual pin output voltage	Compatibility with UUT requirements
d. Resolution	Minimum magnitude of discrete programmable voltage step between values	Programmable function of tester defining voltage level increments available
e. V Swing	Maximum V(logic 1 - V(logic 0)	Defines tester drive voltage capability limits
2. Current Levels a. Drive high	Sourcing output current associated with logic 1	Defines ability of DTU to drive UUT input loads
b. Drive low	Sinking or Sourcing current associated with logic 0	Defines ability of DTU to drive UUT input loads
c. Leakage Hi-Z	Leakage current when driver in tri-state condition	Maximum leakage current UUT must handle from DTU without erratic operation

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
3. Impedance a. Out Drive Hi	Output Impedance for Hi Range Voltage	Impedance matching to UUT through ID
b. Out Drive Lo	Output Impedance for Low Range Voltage	Impedance matching to UUT through ID
c. Output Hi-Z (Off)	Drive in shut-off position	Is impedance high enough to preclude tester loading effects when testing data busses
d. Worst Case Impedance	Identifies minimum Impedance of Output pin	Significant impact to mixed signal applications (Analog/Digital)
D. OPERATIONAL LIMITS 1. Tri_state Drive a. On The Fly Yes[] No[]	Allows drive and sense on the same pin as a function of time	Used for bi-directional lines in real time applications
2. Slew Rates a. Maximum	Inherent Maximum Rise and Fall Times	UUT Requirements, some Flip-Flops may not toggle if too slow
b. Minimum	Inherent Minimum Rise and Fall Times	Provides a rough measure of cross coupling and noise inducement susceptibility
3. Voltages a. Maximum Voltage at maximum rate (UnMultiplexed)	Shows where voltage starts dropping off as data rate increases	Points out realistic limits of what tester can be programmed to.
b. Maximum voltage at maximum data rate (multiplexed)	Shows where voltage starts dropping off as data rate increases	Points out realistic limits of what tester can be programmed to.

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
4. Data Rate Generator a. Has DRG []	Ability to control pattern rates	UUT Requirements
b. Doesn't Have DRG []	Fixed Data Rate imposes severe test capability penalty	UUT Requirements
c. (UnMultiplexed) Minimum Data Rate, External Trigger	Minimum Data Rate when triggered from an external source	Synchronization from other station assets or UUT requirements
d. Minimum Data Rate (UnMultiplexed)	Minimum Data Rate of Tester	Cutoff point where tester can no longer supply output data to UUT
e. Maximum Data Rate (UnMultiplexed)	Maximum Data Rate of Tester	UUT Requirements/Up limit of tester
f. Maximum Data Rate External Trigger (UnMultiplexed)	Maximum Data Rate the tester can provide when externally triggered	Maximum Data Rate Requirements of UUT
g. Maximum Data Rate at Maximum Voltage (UnMultiplexed)	Show where data rate can no longer be increased and still provide maximum voltage	Points out realistic limits tester can be programmed to
h. Resolution	Smallest increment in Data Rate that the tester can be programmed to	Show what tester can be programmed to
i. Accuracy	Data Rate accuracy	Shows how accurately data rate can be programmed to
j. Jitter	Stability of Data Rate	UUT Requirements for stability of data inputs(Rate)

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
k. Min Data Rate External Trigger (Multiplexed)	Minimum Data Rate when triggered from an external source	Synchronization from other station assets or UUT requirements
l. Min Data Rate (Multiplexed)	Minimum data rate of Tester	Cutoff point where tester can no longer supply data output to UUT
m. Maximum Data Rate (Multiplexed)	Maximum Data Rate of Tester	UUT Requirements/Up limit of tester
n. Max Data Rate, External Trigger (Multiplexed)	Maximum Data Rate the tester can provide when externally triggered	Maximum Data Rate Requirements of UUT
o. Maximum Data Rate at Maximum Voltage (Multiplexed)	Show where data rate can no longer be increase and still provide maximum voltage	Points out realistic limits tester can be programmed to
p. Resolution (Multiplexed)	Smallest increment in Data Rate the tester can be programmed to	Show what tester can be programmed to
q. Accuracy (Multiplexed)	Data Rate accuracy	UUT Requirements/Up limit of tester
r. Jitter (Multiplexed)	Stability of Data Rate	UUT Requirements for stability of data rate inputs
E. MEMORY 1. Pin Pattern Memory a. Pin Memory (1) Yes [] (2) No []	Capability of extended hi-speed bursts of patterns	Defines ability of DTU to generate multiple patterns unrestrained by Computer I/O or DMA rates

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
b. Ram Depth	Number of Bits deep of output pin memory	Indicates maximum serial depth of stimulus pattern burst
2. Store Method a. Not Applicable []	Verification of storage behind pin	If no pin memory available, must use Computer I/O or DMA with severe speed restrictions
b. Exp Vs Actual	Capability of performing comparisons with actual vs expected state on-the-fly	Used to improve tester response times(overhead)
c. (1) With Mask [] (2) Without Mask []	Capability of storing results with error flagging or not, pattern by pattern	Used to improve tester response times (overhead)
d. Signature Analysis []	Polynomial Algorithm to store accumulated data/time information	Technique for compressed data/time testing to handle very large numbers of patterns in a test
3. Pattern Generator, Algorithmic (1) []	Capability of generating tests based on pre-stored algorithms	Expands capability of Pin memory without sacrifice of speed
Ram (2) []	Capability of stimulus generation based on pre-stored patterns	Hi-speed stimulus/response capability, limited by Ram speed/depth
Direct (3) []	Latched capability for broadside stimulus generation	Stimulus of multiple pins at same time

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
F. DYNAMIC CHARACTERISTICS 1. Formatter selectable to a. (1) DTU [] (2) CARD [] (3) PIN []	Is this particular pin governed by a format selection to the DTU, Card, or individual pin level	Capability of tester to provide different signal formats on different pins simultaneously or on a card by card, or pin by pin basis or must the entire DTU be a single format for each timing set
b. Types (UnMultiplexed) (1) NR [] (2) R1 [] (3) SBC [] (4) RZ [] (5) RO [] (6) RTC [] (7) DNRZ []	Individual format that can be generated within the DTU for the unmultiplexed mode	Does UUT require a format generated by this particular pin
c. Types (Multiplexed) (1) NR [] (2) R1 [] (3) SBC [] (4) RZ [] (5) RO [] (6) RTC [] (7) DRNZ []	Individual format that can be generated within the DTU for the multiplexed mode	Does UUT require a format generated by this particular pin
2. Timing Gen per a. (1) DTU [] (2) CARD [] (3) PIN []	Specifies if there is a timing generator for each pin, card, or one per DTU	Useful for tester capability comparison and for critical UUT timing requirements
b. Number of Timing Sets	The number of timing sets or time/pin definition templates definable	TPS development for complex digital & hybrid UUTs. Primarily used for bus emulation

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
c. Stimulus Periods per Timing Set	Maximum Number of Stimulus periods in a given timing set	TPS development & interfacing with dynamic or multiplexed data devices
d. Clocks per Timing Set	Maximum number of clocks per pattern for a Timing Set. Value used is an integer value from 1 to the max	Maximum definition of number of clock cycles for a timing set.
e. Pattern Period (1) Min	Minimum time period between leading edges of one pattern to the leading edge of the next pattern	Basic characteristic and limitation of the DTU pulse generation capability
(2) Max	Maximum time period between leading edge of one pattern to leading edge of next pattern	Basic characteristics and limitations of the DTU pulse generation capability
(3) N/A		
(4) Accuracy	Basic accuracy of pulse period over its operating range, specified in percent	Basic characteristics and limitations of the DTU pulse generation capability
f. Stim Period Begin Time (1) Min	Minimum time after T0 when edge of stim pulse begins	Basic characteristic and limitation of the DTU pulse generation capability

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
(2) Max	Maximum time after T0 when stim edge placement can occur	Basic Characteristic and limitation of the DTU pulse generation capability
(3) Res	Edge placement resolution of the leading edge of stim period	Basic capability and limitation of DTU Pulse Generation capability
(4) Acc	Accuracy of placement of leading edge of stim period	Basic capability and limitation of the DTU pulse generation capability
g. Stim Period End T (1) Min	Minimum time after beginning of stim period to allow minimum pulse width	Basic capability and limitation of the DTU pulse generation capability
(2) N/A		
(3) Res	Edge placement resolution of trailing edge of stim pulse	Basic capability and limitation of the DTU pulse generation capability
(4) Acc	Accuracy of Edge Placement of stim training edge pulse	Basic capability and limitation of the DTU pulse generation capability
h. Stim Period Width (1) Min	Minimum pulse width tester can provide	Basic capability and limitation of DTU pulse generation capability
(2) N/A		
(3) N/A		

TABLE 1 - DIGITAL TESTER OUTPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
(4) N/A		
i. Stim Period On/Off (1) N/A		
(2) Max	Maximum pulse decay time from stim ON to true OFF voltage	Used mainly in systems with multiplex timing characteristics and permit design to protect components from undesired timing conflicts
(3) N/A		
(4) N/A		

4.0 DIGITAL TESTER INPUT CHARACTERISTICS

This section covers the specific format developed for the Digital Tester Input Characteristics, see Figure 2. All Testers need to address items A through D. For items not applicable state N/A, just as in Section 3. For memory capability address item E. For Dynamic Requirements address item F. The remainder of the chapter is backup data to support Figure 2, see Table 2.

FIGURE 2 - DIGITAL TESTER INPUT CHARACTERISTICS

GPI PIN NO (S)

INPUT

A Interfacing

1 TYPE
a Single ☐
b I/O ☐
c Dynamic ☐
d Static ☐ ans (1) & (2)

(1) Sequential I/O Strobe
Yes ☐ No ☐

(2) Broadside Capability
Yes ☐ No ☐

2 DELAYS
In nanoseconds

Parameter	Value
a Strobe Skew - Pin/Pin same card	
b Strobe Skew - Pin/Pin different card	
c Ext Trigger in to this pin	
d Delay Inst to I/O	

3 BOUNDARY SCAN
(1)Yes ☐ (2)No ☐

4.
a Shielding
(1) Yes ☐ (2) No ☐
Check only one
b Shielded and grounded at DTU ☐
c Shielded and grounded at I/F ☐
d Coax and grounded at I/F ☐
e Coax and grounded at DTU ☐
f Twisted Pair ☐

B Technologies

Check all that apply

1 TTL		11 CMOS	
2 ALS		12 HC	
3 AS		13 ECL	
4 F		14 ECL 10K	
5 H		15 ECL 10KH	
6 L		16 ECL 100K	
7 LS		17 HYBRID	
8 N		18 OTHER	
9 S		If other specify	
10 MOS			

C DC Levels

1 Level Sets
a No of level sets
b No of thresholds per level set ______

2 Voltage Characteristics

Parameter	Value
a Voltage in High	
b Voltage in Low	
c accuracy	
d Resolution	
e Min Del Ampl	

3 Load Current
Commutative
(a)Yes ☐ (b)No ☐

Parameter	Value
c Logic 1 Current	
d Logic 0 Current	
e Commutating V	

4 Impedance Characteristics
(without Res Load)

Parameter	Value
a Logic 1 Impedance	
b Logic 0 Impedance	

5 Loads (resistive)
(a) Constant ☐
(b) Commutating ☐

Parameter	Value
(1) Logic 1 Resistance	
(2) Logic 0 Resistance	
(3) Commutating V	

D AC Levels

1. Data Rates

Parameter	Value
a Min Data Rate	
b Max Data Rate	
c Resolution	
d Accuracy	
e Jitter	

2. Stray Load Capacitance

Parameter	Value
a Driver Off	
b Driver On	

3. Crosstalk
(between adjacent pins)

Parameter	Value
a Crosstalk	MV
b Max Data Rate	MHZ
c Voltage at Max Data Rate	V

4. Quiescent Noise Level	

E Pin MEMORY

1 Memory Available
(a)yes ☐ (b)no ☐
2. Signature Analysis
(a)yes ☐ (b)no ☐
3 Ram Depth
4 Store Method (data)
Check if Applicable
a Not Applicable ☐
b Exp vs Actual ☐
c Detected State ☐
d With Mask ☐
e Without Mask ☐
5 Store Method (Algorithmic)
a Address ☐
6 Masking on the Fly
(a)Yes ☐ (b)No ☐

F DYNAMIC CHARACTERISTICS

1 Timing Gen
Selectable to

a. DTU ☐ (1)
CARD ☐ (2)
PIN ☐ (3)
b. Timing Sets
c. Window Periods/Set ______

Timing Parameter	(1)Min	(2)Max	(3)Res	(4)Acc
d. Pattern Period				
e. Resp Period Begin T				
f. Resp Period End T				
g. Resp Period Width				
h. Resp Period on/off				

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
A. INTERFACING 1. Type a. Single b. I/O	Address whether pin is single dedicated or bi-directional	To show if a pin is bi-directional; if it can handle busses
c. Static d. Dynamic	Addresses basic capability of tester	Delineates whether tester has can handle time dependent input signal
If Static 1. Sequential I/O Strobe (a) Yes [ ] (b) No [ ]	Address ability of tester to look at returned data	Some older digital testers looked at one DTU card at a time in response mode
2. Broadside Capability (a) Yes [ ] (b) No [ ]	Addresses capability of tester to look at returned data	Addresses the capability of the tester to examine all input pins simultaneously but not time dependent
Delays a. Strobe skew - Pin/Pin (Same Card)	Addresses testers internal delays in reading input data	Required information for TPS design of critical timing requirements
b. Strobe Skew - Pin/Pin (Diff Card)	Addresses testers internal delays in reading input data using different DTU cards	Required information for TPS design of critical timing requirements
c. External Trigger to this pin	External trigger to turn output pin either on or off	Critical timing consideration when DTU requires a response from UUT in a specific time window

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
d. Delay inst to I/O	Delay in nanoseconds between the DTU input and station I/O	A factor to be considered in TPS design when critical timing is a factor
3. Boundary Scan (a) Yes [] (b) No []	Tester specifically does or does not have a boundary scan capability (protocols and deep > 1 meg Memory)	Some newer UUT designs make extensive use of this capability
4. Shielding (1) Yes [] (2) No []	Reduces susceptibility to outside stimulus and interference	Tester would be severely limited to perform adequately above 10 Mhz
b. Shielded and grounded at DTU []	Provides good signal grounding fidelity up to approx. 20 Mhz	Required for shielding design in ID
c. Shielded and grounded at I/F []	Provides good signal grounding fidelity up to approx 20 Mhz	Required for shielding design in ID
d. Coax and grounded at DTU []	Provides good signal grounding fidelity above 20 Mhz up to GHz range	Required for hi-speed signal interconnect to ID
e. Coax and grounded at I/F []	Provides good signal grounding fidelity above 20 Mhz up to Ghz range	Required for hi-speed signal interconnect to ID
f. Twisted Pair []	Inexpensive shielding method valid to approx. 10 Mhz	Required for interconnect matching into ID
B. TECHNOLOGIES	Identifies specific logic characteristics (voltages,currents, impedances)	Identifies specific operating parameters required during testing

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
C. DC LEVELS 1. Level Sets a. No of level Sets	Number of incompatible logic families the DTU can handle at one time	Indicative of logic family and interfacing required
b. No of active thresholds	Either 1 or 2 (Older testers have only one)	Indicative of whether Tri-state logic can be supported
2. Voltage Characteristics a. Vin high	Programmable threshold voltage of logic 1 (Minimum)	Defines the high state sensor comparator voltage threshold
b. Vin low	Programmable threshold voltage of logic 0 (Maximum)	Defines the low state sensor comparator voltage threshold
c. Accuracy	Accuracy of comparators & DAC that provide Ref voltages	Compatibility with UUT requirements for accuracy
d. Resolution	Minimum increment to which a threshold can be programmed	Programmable function of tester
e. Minimum Detectable Amplitude	Minimum detectable voltage the tester can sense	Measure of comparator sensitivity
3. Load Current Commutative a. Yes [] b. No [] if No, answer c & d	Specifies whether load current is switched as a function of logic state	This function may be needed in ID if load current is not commutative
c. Logic 1 Current Value	Sinking or Sourcing current associated with logic 1	Determine if UUT has sufficient drive capability (reduces UUT noise margin if not)

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
d. Logic 0 Current Value	Sinking or Sourcing current associated with logic 0	Determine if UUT has sufficient drive or sinking capability
e. Commutating Voltage	Threshold for load current switching	Required to emulate in-system UUT requirements. If not, may be required in ID
4. Impedance Characteristics (without Res Load) a. Logic 1 Impedance	Impedance imposed when logic 1 sensed	Load impedance greater than 100K ohms for good interface compatibility with UUT
b. Logic 0 Impedance	Impedance imposed when logic 0 sensed	Load impedance greater than 100K ohms for good interface compatibility with UUT
5. Loads (Resistive) (a) Constant []	Single resistive load per pin, sometimes in personality module	Not preferable
(b) Commutative []	Two selectable resistance load levels per pin, sometimes in personality module	Matching UUT drive capability
(1) Logic 1 Resistance	Load Resistance with sensed logic 1	Proper UUT loading
(2) Logic 0 Resistance	Load Resistance with sensed logic 0	Proper UUT loading
(3) Commutating Voltage	Programmable voltage threshold at which the resistance is switched	Applicable for commutative resistance loading only

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
D. AC LEVELS 1. Data Rates a. Min Data Rate	Minimum data rate tester can support	Minimum data rate UUT must supply tester
c. Max Data Rate	Maximum data rate tester can support	Maximum data rate that UUT must not exceed without active ID buffering
d. Resolution	Smallest increment in Data Rate that the tester can be programmed to	UUT Compatibility
e. Accuracy	Data Rate Accuracy	UUT Compatibility
f. Jitter	Amount of jitter the tester can tolerate	UUT requirements for stability of data inputs(Rate)
2. Stray Load Capacitance a. Driver OFF	Extra unwanted loading	Erroneous data at input caused by tester loading if parameter is too large
b. Driver ON	Extra unwanted loading	Erroneous data at input caused by tester loading if parameter too large
3. Crosstalk (between adjacent pins) a. Crosstalk	Stray voltage from adjacent pins at max data rate & Maximum Swing	Erroneous data rate at input to tester. Decreases noise margin
b. Max Data Rate	Maximum data Rate the tester can provide	Condition when crosstalk is measured

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
c. Voltage swing at Max Data Rate	Maximum voltage swing at maximum data rate	Condition when Crosstalk is measured after data rate is achieved
4. Quescent Noise Level	Number of bits of depth of input memory.	Affects Noise margin between actual logic family and voltage thresholds
E. PIN MEMORY 1. Memory available (a) Yes [] (b) No []	Capability of extended hi-speed bursts of patterns	Defines ability of DTU to generate multiple patterns unrestrained by Computer I/O or DMA rates
2. Signature Analysis (a) Yes [] (b) No []	Polynomial Algorithm to store accumulated data/time information	Technique for compressed data/time testing to handle very large numbers of patterns
3. Ram Depth	Number of bits of depth of input memory.	Maximum number of patterns in a burst without algorithmic aid
4. Store Method a. Not Applicable []	Verification of data storage behind pin	If no pin memory available, must use computer I/O or DMA with severe speed restrictions
b. Exp vs Actual []	Capability of performing comparisons with actual vs expected state on-the-fly	Used to improve tester response times (reduce overhead)
c. Detected State []	Stores detected state without pass/ fail	Used with multiple pins for ranging

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)

CATEGORY	FUNCTION	REQUIREMENT/REASON
d. With Mask []	Capability of storing results with error flagging, pattern by pattern	Used to improve tester response times (computer overhead)
e. Without Mask []	Capability of storing results without error flagging, pattern by pattern	Useful for debugging UUTs
5. Store Method (Algorithmic) a. Address []	Capability of generating tests based on pre-stored algorithms	Expands capability of Pin memory without sacrifice of speed
6. Masking on the Fly (a) Yes [] (b) No []	Capability of mask modification on-the-fly, without impacting data rates	UUT Requirements
F. DYNAMIC CHARACTERISTICS 1. Timing Generator selectable to a. (1) DTU [] (2) CARD [] (3) PIN []	Is this particular pin governed by a timing selection to the DTU, Card, or individual pin level	Capability of tester to provide different signal timing on different pins simultaneously or on a card by card, or pin by pin basis or must the entire DTU be a single timing set
b. Number of Timing Sets per set	Maximum number of timing sets or time/pin definition templates definable	TPS development for complex digital & hybrid UUTs. Primarily used for bus emulation
c. Response Periods per Timing Set	Maximum Number of Response periods in a timing set	TPS development & interfacing with dynamic or multiplexed data devices

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
e. Pattern Period (1) Min	Minimum time period between leading edges of one Response time of the beginning edge of the next response or stimulus event	Basic characteristic and limitation of the DTU timing capability
(2) Max	Maximum time period between beginning of one pattern to the beginning of the next pattern	Basic characteristics and limitations of the DTU timing capability
(3) N/A		
(4) Accuracy	Basic accuracy of pattern period over its operating range, specified in percent	Basic characteristics and limitations of the DTU timing capability
f. Resp. Period Begin Time (1) Min	Minimum time after T0 when edge of Response period begins	Basic characteristic and limitation of the DTU timing capability
(2) Max	Maximum time after T0 when Response ending can occur	Basic Characteristic and limitation of the DTU timing generation capability
(3) Res	Placement resolution of the Response period leading edge	Basic capability and limitation of DTU timing capability
(4) Acc	Accuracy of placement of the beginning of the Response period	Basic capability and limitation of the DTU timing capability

TABLE 2 - DIGITAL TESTER INPUT CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
g. Resp Period End T (1) Min	Minimum time after beginning of Response period to allow minimum width	Basic capability and limitation of the DTU timing capability
(2) N/A	Edge placement accuracy of Response Period ending	Basic capability and limitation of the DTU timing capability
(3) Res	Edge placement resolution of trailing edge of Response period	Basic capability and limitation of the DTU timing capability
(4) Acc	Accuracy of Edge Placement of Response ending time	Basic capability and limitation of the DTU timing capability
h. Resp Period Width (1) Min	Minimum Response width tester can Respond consistently to	Basic capability and limitation of DTU timing capability
(2) N/A		
(3) N/A		
(4) N/A		
i. Resp Period On/Off (1) Min	Define minimum time period between Response periods within pattern	Basic capability and limitation of DTU timing capability
(2) N/A		
(3) N/A		
(4) N/A		

5.0 DIGITAL TESTER CLOCK CHARACTERISTICS

This section covers the specific format to be used for external clock line(s) coming into the tester and clock line(s) coming from the tester to other units, see Figure 3. All of the items, A through D in Figure 3 are required to be addressed. The remainder of the chapter, see Table 3, is backup data that supports all of the items addressed in this section.

FIGURE 3 - DIGITAL TESTER CLOCK CHARACTERISTICS

GPI PIN NO(S)

A — INTERFACING

1. Signal Name ______________

2. Direction
   - a Input ☐
   - b Output ☐
   - c Bi-directional ☐

3. Shielding
   - a Shielded
     - (1) Yes ☐
     - (2) No ☐

   Check only one

   - b Shielded and grounded at DTU ☐
   - c Shielded and grounded at I/F ☐
   - d Coax and grounded at DTU ☐
   - e Coax and grounded at I/F ☐
   - f Twisted Pair ☐

B — TECHNOLOGY

1. TTL	
2. ALS	
3. AS	
4. F	
5. H	
6. L	
7. LS	
8. N	
9. S	
10. MOS	
11. CMOS	
12. HC	
13. ECL	
14. ECL 10K	
15. ECL 10KH	
16. ECL 100K	
17. BIPOLAR	
18. HYBRID	
OTHER	
	/

C — DC LEVELS

Parameter	Value
Voltage High	
Voltage Low	
Accuracy	

D — AC Levels

Parameter	Value
Minium Freq	
Max Freq	
Risetime	
Falltime	
Jitter	

TABLE 3 - DIGITAL TESTER CLOCK LINE CHARACTERISTICS

CATEGORY	FUNCTION	REQUIREMENT/REASON
A. INTERFACING 1. Signal Name		
2. Signal Type a. Single Ended [] b. Differential []	Define type of interface used, whether single ended referenced to ground, or differential, referenced to each other	Determines ID requirements for use
3. Direction a. Input [] b. Output [] c. Bi-Direct -ional []	Determine control of asynchronism; by Tester or UUT	As input, Clocking provides external control for Tester, as output, Clocking provides control over UUT
4. Shielding a. Shielded (1) Yes [] (2) No []	Reduces susceptibility to outside stimulus and interference	Tester would be severely limited to perform adequately above 10 Mhz
b. Shielded and grounded at DTU []	Provides good signal grounding fidelity up to approx. 20 Mhz	Required for shielding design in ID
c. Shielded and grounded at I/F []	Provides good signal grounding fidelity up to approx 20 Mhz	Required for shielding design in ID
d. Coax and grounded at DTU []	Provides good signal grounding fidelity above 20 Mhz up to GHz range	Required for hi-speed signal interconnect to ID
e. Coax and grounded at I/F []	Provides good signal grounding fidelity above 20 Mhz up to Ghz range	Required for hi-speed signal interconnect to ID

TABLE 3 - DIGITAL TESTER CLOCK LINE CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
f. Twisted Pair []	Inexpensive shielding method valid to approx. 10 Mhz	Required for interconnect matching into ID
B. TECHNOLOGY	Identifies specific logic characteristics (voltages,currents, impedances)	Identifies specific operating parameters required during testing
C. DC LEVELS 1. Voltage High	Defines Tester High logic state voltage range, as minimum threshold	Define High state threshold for Clock signals
2. Voltage Low	Defines Tester Low logic state voltage range, as maximum threshold	Define Low state threshold for Clock signals
3. Accuracy	For Clock outputs, defines percent accuracy of programmed or preset values	Required for ID design.
D. AC LEVELS 1. Minimum Frequency	Lowest Clock rate at which tester can function reliably	UUT Requirements
2. Maximum Frequency	Maximum Clock rate at tester can function reliably	UUT Requirements
3. Rise time	Determine rough susceptibility to noise and stray coupling	UUT Requirements
4. Falltime	Determine rough susceptibility to Noise and stray coupling	UUT Requirements

TABLE 3 - DIGITAL TESTER CLOCK LINE CHARACTERISTICS (CONT)		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
5. Jitter	Defines stability of clock signal	Required for UUt/Tester compatibility analysis

6.0 DIGITAL TESTER CONTROL LINE CHARACTERISTICS

This section covers the specific format to be used for external control line(s) coming into the tester from an outside source or originating from the tester going to some outside source. All items, A through D in Figure 4 require to be addressed. The remainder of this chapter is backup data that supports all of the elements in this section.

FIGURE 4 – DIGITAL TESTER CONTROL LINE CHARACTERISTICS

GPI PIN NO(S)

A INTERFACING

1. Signal Name ______

2. Direction
   - a Input ☐
   - b Output ☐
   - c Bi-directional ☐

3. Shielding
   - a Shielded
     - (1) Yes ☐
     - (2) No ☐

   Check only one

   - b Shielded and grounded at DTU ☐
   - c Shielded and grounded at I/F ☐
   - d Coax and grounded at DTU ☐
   - e Coax and grounded at I/F ☐
   - f Twisted Pair ☐

B TECHNOLOGY

1. TTL	
2. ALS	
3. AS	
4. S	
5. [illegible]	
6. H	
[illegible]	
7. LS	
8. N	
9. S	
10. MOS	
11. CMOS	
12. HC	
13. ECL	
14. ECL 10K	
15. ECL 10KH	
16. ECL 10CK	
17. BIPOLAR	
18. HYBRID	
OTHER	
19.	

C DC LEVELS

Parameter	Value
1. Volt High Safe	
2. Volt Low Safe	
3. Volt High Operate	
4. Volt Low Operate	

5. Active:
   (a) High ☐ (b) Low ☐

D TIMING

Parameter	Value
1. Minium Initiate Time	
2. Minium Release Time	

TABLE 4 - DIGITAL TESTER CONTROL LINE CHARACTERISTICS		
CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
A. INTERFACING 1. Signal Name		
2. Signal Type a. Single Ended [ ] b. Differential [ ]	Define type of interface used, whether single-ended referenced to ground, or, differential, referenced to each other	Determines Interface Device (ID) requirements for use
3. Direction a. Input [ ] b. Output [ ] c. Bi-Direct -ional [ ]	Determine control of asynchronism; by Tester or UUT	As input, provides external control for Tester, as output, controls UUT in relation to Tester
4. Shielding a. Shielded (1) Yes [ ] (2) No [ ]	Reduces susceptibility to outside stimulus and interference	Tester would be severely limited to perform adequately above 10 Mhz
b. Shielded and grounded at DTU [ ]	Provides good signal grounding fidelity up to approx 20 Mhz	Required for shielding design in ID
c. Shielded and grounded at I/F [ ]	Provides good signal grounding fidelity up to approx 20 Mhz	Required for shielding design in ID
d. Coax and grounded at DTU [ ]	Provides good signal grounding fidelity above 20 Mhz up to GHz range	Required for hi-speed signal interconnect to ID
e. Coax and grounded at I/F [ ]	Provides good signal grounding fidelity above 20 Mhz up to Ghz range	Required for hi-speed signal interconnect to ID
f. Twisted Pair [ ]	Inexpensive shielding method valid to approx 10 Mhz	Required for interconnect matching into ID

TABLE 4 - DIGITAL TESTER CONTROL LINE CHARACTERISTICS (CONT)

CATEGORY	**FUNCTION**	**REQUIREMENT/REASON**
B. TECHNOLOGY	Identifies specific logic characteristics (voltages,currents, impedances)	Identifies specific operating parameters required during testing
C. DC LEVELS 1. Volt High Safe	Most positive voltage pin can handle without damage	UUT/ID Requirements
2. Volt Low Safe	Most negative voltage pin can handle without damage	UUT/ID Requirements
3. Volt High Operate	Define High state threshold (minimum) or drive output	UUT/ID Requirements
4. Volt Low Operate	Define low state threshold (maximum) or drive output	UUT/ID Requirements
5. Active (a) High (b) Low	Defines True (asserted state) of signal	UUT/ID Requirements
D. TIMING 1. Min Initiate Time	Minimum time required before critical event to initiate control this signal is designed for	UUT/ID Requirements
2. Min Release Time	Minimum time required to release control from signal going false edge	UUT/ID Requirements

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INTENTIONALLY

7.0 FINDINGS

a. Considerable research of Government and Commercial Activities did not produce formats already developed that could be used. There are some parametric data bases in existence that were found but they do not go to the level of detail that is necessary for a true "Hardware Congruent" comparison.

b. In test equipment specifications, the same terminology means something slightly different from contractor to contractor. These slight but ambiguous differences make comparisons of testers, based on present specifications very difficult.

c. There was a continual conflict between the totality of all possible parameters versus what was significant. Among those parameters considered significant there was a conflict between what was practicable to obtain, using test equipment at the pin interface, and what was not. For those parameters that were significant but very difficult to obtain other indirect methods were required such as lumped parameters.

8.0 CONCLUSIONS

a. Although a considerable effort has gone into the generation of these formats they cannot cover all possible capabilities for all Digital Board/Assembly testers that could be encountered. However they should cover enough of all pertinent data to get either a "Congruent" or a very close match between tester capabilities at the Hardware Interface Level.

b. This effort represents the first serious effort at trying to standardize electronic hardware interface specification for testers.

9.0 RECOMMENDATIONS

Before attempting to use the formats provided in this report get a clear understanding of the terminology used in the subject tester to be "Formatted" and reconcile those definitions with those contained in the Glossary of this report.

APPENDIX A

The following pages contain examples of the four different types of formats contained in this report. These formats are:

(a) Digital Tester Output Characteristics

(b) Digital Tester Input Characteristics

(c) Digital Tester Clock Characteristics

(d) Digital Tester Control Line Characteristics

DIGITAL TESTER OUTPUT CHARACTERISTICS

GPI PIN NO (S)

OUTPUT

A — INTERFACING

1. TYPE
   - a. Single ☐
   - b. I/O ☐
   - c. Dynamic ☐
   - d. Static ☐

2 Delays in nanoseconds

Parameter	Value
a. Skew - Pin/Pin same card	
b. Skew - Pin/Pin different card	
c. Gated Clock Out This Pin	
d. Ext Clock In to This Pin	
e. Ext Trigger In to This Pin	
f. Delay Inst to I/O	

3 Shielding

a. Shielding
- (1) Yes ☐
- (2) No ☐

Check only one

- b. Shielded and grounded at DTU ☐
- c. Shielded and grounded at I/F ☐
- d. Coax and grounded at DTU ☐
- e. Coax and grounded at I/F ☐
- f. Twisted Pair ☐

4 Boundary Scan

a. Yes ☐ b. No ☐

B — TECHNOLOGIES

Check all that apply

		OTHER	
1 TTL			
2 ALS		19	
3 AS		20	
4 F		21	
5 H		22	
6 L		23	
7 LS		24	
8 N		25	
9 S		26	
10 MOS		27	
11 CMOS		28	
12 HC		29	
13 ECL		30	
14 ECL 10K		31	
15 ECL 10KH		32	
16 ECL 10CK			
17 BIPOLAR			
18 HYBRID			

C — DC LEVELS

1. Voltage Levels

Parameter	Value
a High Range	
(1) V Out High	
(2) V Out Low	
b Low Range	
(1) V Out High	
(2) V Out Low	
c. Accuracy	
d Resolution	
e. V Swing	

2. Current Levels

Parameter	Current
a. Drive Hi	
b. Drive Lo	
c. Leakage Hiz	

3. Impedance

Parameter	Imp
a. Out Drive Hi	
b. Out Drive Lo	
c. Out Hiz (off)	
d. Worse Case	

D — OPERATIONAL LIMITS

1 Tri-State Drive	Yes	NO
a. On The Fly		

2. Slew Rates	
a Maxium	
b. Minium	

3 Voltages	
a. Max Voltage at Max Data Rate (unmultiplexed)	
b. Max Voltage at Max Data Rate (multiplexed)	

4 Data Rate Gen	
a Has DRG	
b. Doesn't have DRG	
Parameter (unmultiplexed)	
c. Minium Data Rate External Trigger	
d. Minium Data Rate	
e. Max Data Rate	
f. Max Data Rate External Trigger	
g. Max Data Rate at Max Voltage	
h Resolution	
i Accuracy	
j Jitter	
Parameter (multiplexed)	
k. Minium Data Rate External Trigger	
l Minium Data Rate	
m Max Data Rate	
n. Max Data Rate External Trigger	
o. Max Data Rate at Max Voltage	
p Resolution	
q Accuracy	
r Jitter	

E — MEMORY

1 Pin Pattern Memory
- a Pin Memory yes ☐ no ☐
- b Ram Depth

2 Store Method
- a Not Applicable ☐
- b Exp vs Actual (1) ☐
  - Detected State (2) ☐
- c With Mask (1) ☐
  - Without Mask (2) ☐
- d Signature Analysis (3) ☐

3 Pattern Generator
- Algorithmic (1) ☐
- a Ram (2) ☐
- Direct (static only) (3) ☐

F — DYNAMIC CHARACTERISTICS

1 Formatter selectable to
- a. DTU ☐ (1)
- CARD ☐ (2)
- PIN ☐ (3)

b. Types (unmultiplexed)
- NR ☐ (1)
- RI ☐ (2)
- SBC ☐ (3)
- RZ ☐ (4)
- RO ☐ (5)
- RTC ☐ (6)

c Types (multiplexed)
- NR ☐ (1)
- RI ☐ (2)
- SBC ☐ (3)
- RZ ☐ (4)
- RO ☐ (5)
- RTC ☐ (6)

2 Timing Gen
Due for each
- a. DTU (1)
- CARD (2)
- PIN (3)

b. Timing Sets ____________

c Stimulus /periods/set

d Clocks per set

Timing Parameter	(1)Min	(2) Max	(3)Res	(4)Acc
e Pattern Period				
f. Stim Period Begin				
g Stim Period End				
h Stim Period Width				
i. Stim Period on/off				

DIGITAL TESTER INPUT CHARACTERISTICS

GPI PIN NO (S)

INPUT

A Interfacing

1 TYPE

a Single ☐
b I/O ☐

c Dynamic ☐
d Static ☐ ans (1) & (2)

(1) Sequential I/O Strobe
Yes ☐ No ☐

(2) Broadside Capability
Yes ☐ No ☐

2 DELAYS in nanoseconds Parameter	Value
a Strobe Skew - Pin/Pin same card	
b Strobe Skew - Pin/Pin different card	
c Ext Trigger in to this pin	
d Delay Inst to I/O	

3. BOUNDARY SCAN
(1)Yes ☐ (2)No ☐

4.
a Shielding
(1) Yes ☐ (2) No ☐
Check only one
b Shielded and grounded at DTU ☐
c Shielded and grounded at I/F ☐
d Coax and grounded at I/F ☐
e Coax and grounded at DTU ☐
f Twisted Pair ☐

B Technologies

Check all that apply

1 TTL		11 CMOS	
2 ALS		12 HC	
3 AS		13 ECL	
4 F		14 ECL 10 K	
5 H		15 ECL 10 KH	
6 L		16 ECL 100K	
7 LS		17 HYBRID	
8 N		18 OTHER	
9 S		If other specify	
10 MOS			

C DC Levels

1 Level Sets
a No of level sets
b No of thresholds per level set ______

2 Voltage Characteristics Parameter	Value
a Voltage in High	
b Voltage in Low	
c accuracy	
d Resolution	
e Min Det Ampl	

3 Load Current Commutative
(a)Yes ☐ (b)NO ☐

Parameter	Value
c Logic 1 Current	
d Logic 0 Current	
e Commutating V	

4 Impedance Characteristics (without Res Load)

Parameter	Value
a Logic 1 Impedance	
b Logic 0 Impedance	

5 Loads (resistive)
(a) Constant ☐
(b) Commutating ☐

Parameter	Value
(1) Logic 1 Resistance	
(2) Logic 0 Resistance	
(3) Commutating V	

D AC Levels

1. Data Rates

Parameter	Value
a Min Data Rate	
b Max Data Rate	
c Resolution	
d Accuracy	
e Jitter	

2. Stray Load Capacitance

Parameter	Value
a Driver Off	
b Driver On	

3. Crosstalk (between adjacent pins)

Parameter	Value
a Crosstalk	MV
b Max Data Rate	MHZ
c Voltage at Max Data Rate	V

4. Quiescent Noise Level	

E PIN MEMORY

1 Memory Available
(a)yes ☐ (b)no ☐
2. Signature Analysis
(a)yes ☐ (b)no ☐
3. Ram Depth
4 Store Method (data)
Check if Applicable
a Not Applicable ☐
b Exp vs Actual ☐
c Detected State ☐
d With Mask ☐
e Without Mask ☐
5 Store Method (Algorithmic)
a Address ☐
6 Masking on the Fly
(a)Yes ☐ (b)No ☐

F DYNAMIC CHARACTERISTICS

1. Timing Gen
Selectable to

a. DTU ☐ (1)
CARD ☐ (2)
PIN ☐ (3)
b. Timing Sets
c. Window Periods/Set ______

Timing Parameter	(1)Min	(2)Max	(3)Res	(4)Acc
d. Pattern Period				
e. Resp Period Begin T				
f. Resp Period End T				
g. Resp Period Width				
h. Resp Period on/off				

DIGITAL TESTER CLOCK CHARACTERISTICS

GPI PIN NO(S)

A INTERFACING

1. Signal Name

____

2. Direction
   - a Input ☐
   - b Output ☐
   - c Bi-directional ☐

3. Shielding
   - a Shielded
     - (1) Yes ☐
     - (2) No ☐

   Check only one

   - b Shielded and grounded at DTU ☐
   - c Sheilded and grounded at I/F ☐
   - d Coax and grounded at DTU ☐
   - e Coax and grounded at I/F ☐
   - f Twisted Pair ☐

B TECHNOLOGY

1. TTL	
2. ALS	
3. AS	
4. E	
5. H	
6. L	
7. LS	
8. N	
9. S	
10. MOS	
11. CMOS	
12. HC	
13. ECL	
14. ECL 10K	
15. ECL 10KH	
16. ECL 10CK	
17. BIPOLAR	
18. HYBRID	
OTHER	

C DC LEVELS

Parameter	Value
Voltage High	
Voltage Low	
Accuracy	

D AC Levels

Parameter	Value
Minium Freq	
Max Freq	
Risetime	
Falltime	
Jitter	

GPI PIN NO(S)

DIGITAL TESTER CONTROL LINE CHARACTERISTICS

A INTERFACING

1. Signal Name

2. Direction
   - a Input ☐
   - b Output ☐
   - c Bi-directional ☐

3. Shielding
   - a Shielded
     - (1) Yes ☐
     - (2) No ☐

   Check only one

   - b Shielded and grounded at DTU ☐
   - c Sheilded and grounded at I/F ☐
   - d Coax and grounded at DTU ☐
   - e Coax and grounded at I/F ☐
   - f Twisted Pair ☐

B TECHNOLOGY

1. TTL	
2. ALS	
3. AS	
4. E	
5. H	
6. L	
7. LS	
8. N	
9. S	
10. MOS	
11. CMOS	
12. HC	
13. ECL	
14. ECL 10K	
15. ECL 10KH	
16. ECL 10CK	
17. BIPOLAR	
18. HYBRID	
OTHER	
19.	

C DC LEVELS

Parameter	Value
1. Volt High Safe	
2. Volt Low Safe	
3. Volt High Operate	
4. Volt Low Operate	

5. Active
   (a) High ☐ (b) Low ☐

D TIMING

Parameter	Value
1. Minium Initate Time	
2. Minium Release Time	

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GLOSSARY OF TERMS

TERM	DEFINITION
Broadside	Static technique drive/ sense technique where all required values for an entire pattern are loaded without regard to their final timing order, and then input/output simultaneously with a single strobe.
Burst	A contiguous sequence of patterns applied to the unit under test (ususally at high data rates) using data previously stored in a pattern memory.
CPP Value	Integer number of clocks per pattern.
CrossTalk	The Crosstalk parameter included in the DTU section is performed by driving a pin at the maximum data rate and its maximum voltage swing as a square wave, at the selected impedance, and measuring the induced voltage on the adjacent (Victim) pin.
Driver	The portion of the DTU that provides the stimulus for a given pin.
Dynamic DTU Mode	Defines single or multiple edges and or response periods per pin per pattern, with quescent state being part of or external to data pattern.

GLOSSARY OF TERMS (CONT)

TERM	DEFINITION
Force	The act of driving a pin to a specified level of current or voltage.
Format(Data)	Definition of type of control of quescent driver pin state outside of Stimulus periods.
Initiate Time	Time required between initiation of a control signal and the related significant signal it references.
Loads:	
Constant Resistive	Constant fixed resistive load applied irrespective of logic state.
Commutative	Load level selected as a function of the logic state of the pin.
Resistive:	
Logic Zero Load	Resistive load applied when pin voltage is less than Commutating Voltage.
Logic One Load	Resistive load applied when pin voltage is greater than Commutating voltage.
(Load switches at Commutating Voltage)	
Constant Current	Constant current load irrespective of pin voltage.
Commutative Current	
Logic Zero Load	Current load applied when pin voltage is less than Commutuative voltage.

GLOSSARY OF TERMS (CONT)

TERM	DEFINITION
Logic One Load	Current load applied when pin voltage is greater than Commutative voltage.

(Load Switches at Commutating Voltage)

Masking or Ignore	Define pin or group of pins whose state is NOT to be compared until otherwise commanded.
Maximum Cycle Time	Max Clock Period or slowest pattern time.
Maximum Burst Length	Maximum number of patterns the test system is capable of executing at sustained data rates.
Maximum Windows	Maximum number of window or response periods programmable during a TSET.
Minimum Cycle Time	Min Clock Period or fastest pattern time.
Minimum Window Time	Minimum window duration possible.
NR	Non-Return, or continuation of programmed state at the end of any defining stimulus period.
Number of Timing Sets	Maximum number of TSETS available for a specific test system.
Pattern Period	Programmable pattern time

GLOSSARY OF TERMS (CONT)

TERM	DEFINITION
Quiescent Noise Level	Noise level present on a Response line (driver off) with all other drivers in the "0" state.
RO	Return the pin to the Open (Off) state at the end of any defining stimulus period.
R1	Return to 1, return the pin state to a logic one (High) at the end of any defining stimulus period.
Release Time	Time required between release of a control signal to its' quiesent state and system response
Response, Sensor	The portion of the DTU that provides the digital measurement capability for a pin.
Response Period On/Off	Minimum time between Response periods within a Timing Set.
RTC	Return the pin to the logical complement of the defined state at the end of any defining stimulus period.
RZ	Return the pin to the zero(low) at the end of any defining stimulus period.
SBC	Surround by complement, similar to RTC, except in effect from preceding T0Clk to the next T0Clk.

GLOSSARY OF TERMS (CONT)

TERM	DEFINITION
Sequential	Static mode drive/sense technique where data is directly input/output from each card as commanded by computer input/output instructions.
Skew	Variation in event timing at the DTU, between measured pins whose time programming is identical.
Static DTU Mode	Only one edge defineable per applicable pin, per pattern, with response not time critical.
Stimulus Period	Programmable period during which assigned pins are set to the defined state.
Stimulus Period Begin Time	Programmable time relative to cycle or clock defining start of defined state drive.
Stimulus Period End Time	Programmable time relative to cycle or clock, defining end of defined state drive and return to chosen format level.
TOPAT	Pulse defining the beginning of each Pattern. Used in determining time placement of stimulus and response windows within a pattern.

GLOSSARY OF TERMS (CONT)

TERM	DEFINITION
Timing Set (TSET)	Pattern cycle timing definition, as a template for signal driving/ sensing as defined in individual patterns. Switchable on-the-fly.
VIH	Driver Voltage level for High state.
VIL	Driver Voltage level for Low state.
VOH	Minimum Sensor Voltage threshhold for high (1) state detection.
VOL	Maximum Sensor Voltage threshhold for low (0) state detection.
Window	Definition of timing for response measurement during dynamic mode operation.
Window Begin Time	Enables data sensing
Window End Time	Programmable end time of response measurement relative to cycle or clock parameter such as leading or training edge.

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